SENSORVIEW

Datasheet

S60HVV01

Including a guidance for

- PCB Footprint for single and dual placement
- Stack-up _ FR4 1T 4layer

Document name	DS_S60HVV01_vA1
Date	14-Sep-2020
Version (revision)	A1
Confidential level	N/A

Overview

- Antenna beam radiating vertically
- Linear polarization

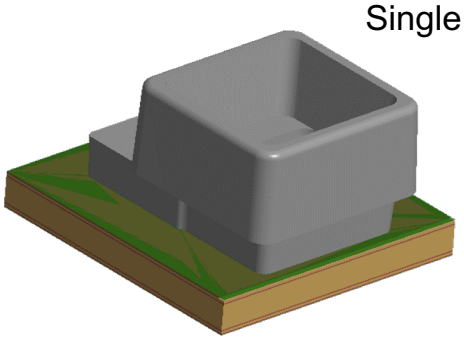
Specification

Frequency range [GHz]	57-66
Typical Far-Field Directivity [dBi]	≥ 8
Polarization	Linear
Return loss [dB]	≤ -10
Nominal impedance [Ω]	50

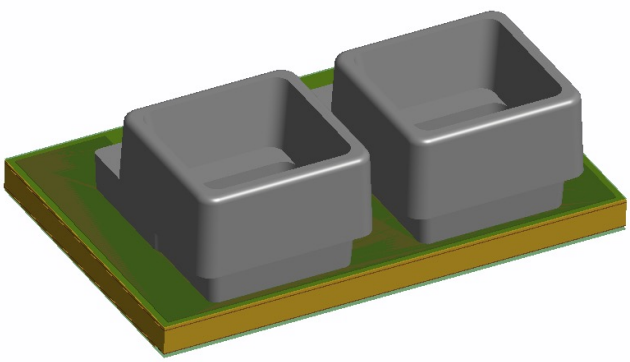
Modeling

[Horn antenna on PCB]

Single



Dual



PCB information

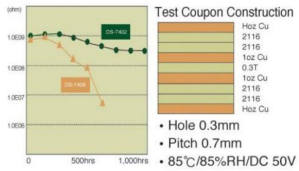
Layer	Lay-Up Structure	Expected Thick(μm)	Copper Ratio	Impedance Pattern Type	Pattern Width	Pattern Space	Target Zo(Ω)
01	1/3 Oz	40 μm	100%				
	1080 62%	65.8 μm		Er : 4.4			
02	1 Oz	31 μm	80%				
	0.7T 1/1	700 μm		Er : 4.4			
03	1 Oz	31 μm	80%				
	1080 62%	65.8 μm		Er : 4.4			
04	1/3 Oz	40 μm	100%		78 μm	222 μm	100 Ω
		or	100%		95 μm		50 Ω

※ NOTE 1:
1. Prepreg thickness specified above are estimated by the loss of etching copper.
2. Final thickness, unless otherwise specified, is to be measured from top copper to bottom copper
3. Minimum data spacing is to be .0035mils(90μm) on inner layers and .004mils(100μm) on outer layer.
4. This stackup can be changed when it cannot be adaptable to your data.

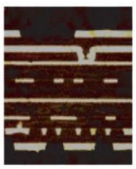
DS-7402
(ANSI: FR-4) Halogen-Free

General Properties

● CAF Resistance Test Result



● Lead-free Soldering Test Result



- Test Condition
  - 8L PCB
  - THB (30℃,RH60%) 168hr→Reflow 260℃ 3 cycles→TCT 100 cycles (-65℃↔125℃)
  - Test Result
  - No delamination
  - No crack

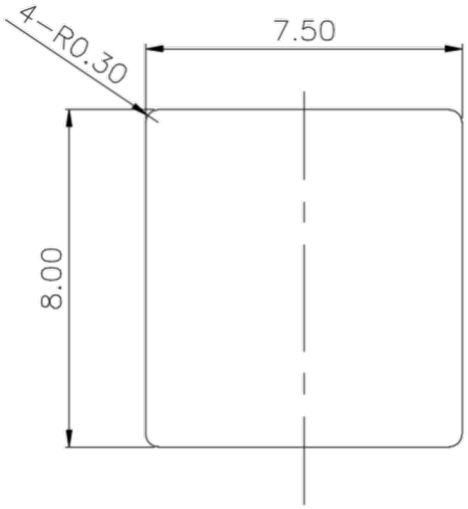
Property	Unit	Test Condition	Typical Value	Test Method
Tg	℃	DSC	150	IPC-TM-650.2.4.25c
		TMA	150	IPC-TM-650.2.4.24c
CTE Z-axis	ppm/℃	Ambient to Tg	45	IPC-TM-650.2.4.41
Z-axis Expansion	%	50℃ to 260℃	3.0	IPC-TM-650.2.4.41
Decomposition Temperature (5% wt loss)	℃	TGA	370	IPC-TM-650.2.3.40
T-260	min	TMA	120	IPC-TM-650.2.4.24.1
T-288	min	TMA	> 60	IPC-TM-650.2.4.24.1
Dielectric Constant (Resin Content 50%)		C-24/23/50 (1GHz)	4.4	IPC-TM-650.2.5.5.9
Dissipation Factor (Resin Content 50%)		C-24/23/50 (1GHz)	0.014	IPC-TM-650.2.5.5.9
Peel Strength (Standard profile 1oz)	N/mm	Condition A	1.6	IPC-TM-650.2.4.8
Water Absorption	%	E-24/50+D-24/23	0.13	IPC-TM-650.2.6.2.1

* IPC-4101B/92 * Test specimen thickness: 1.0mm (7628x5)

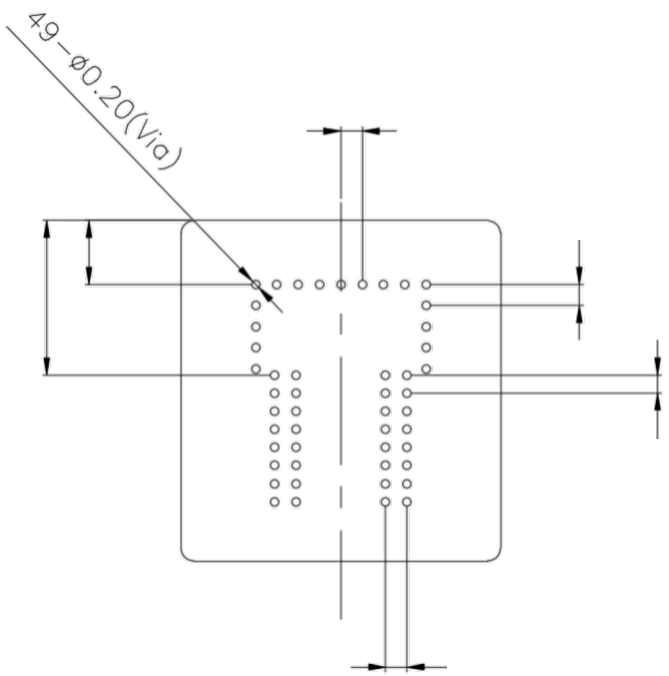
[Source: http://www.doosanelectronics.com/download/pdf/catalog/DS-7402.pdf]

PCB layer (Single)

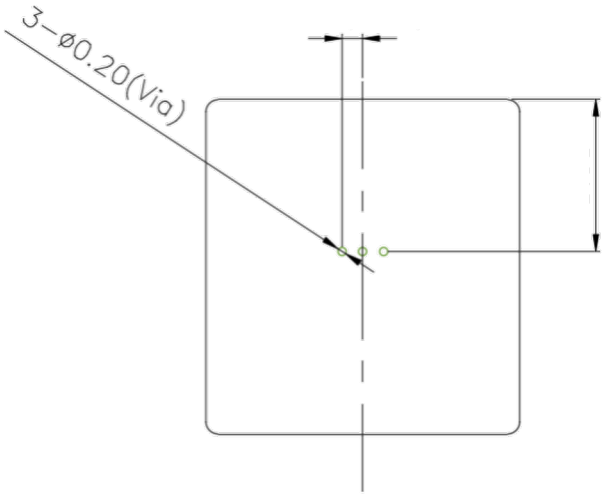
■ Contour



■ Via Hole (Layer 1 ~ Layer 4)

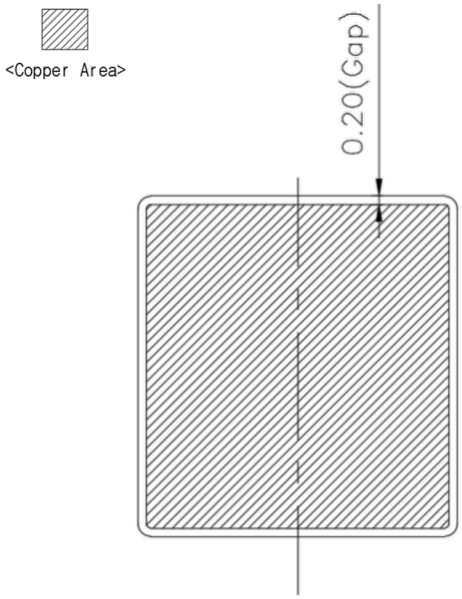


■ Via Hole (Layer 2 ~ Layer 3)

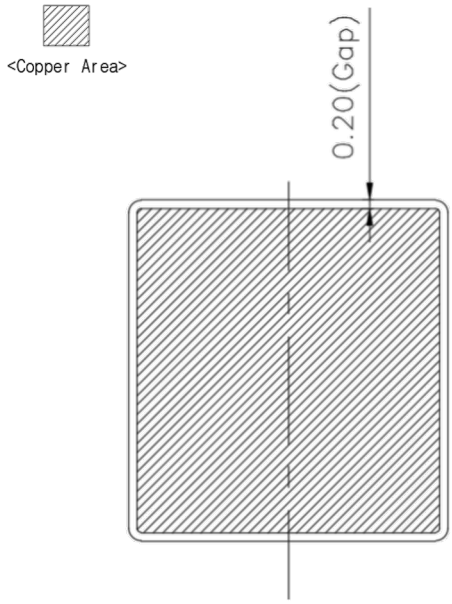


PCB layer (Single)

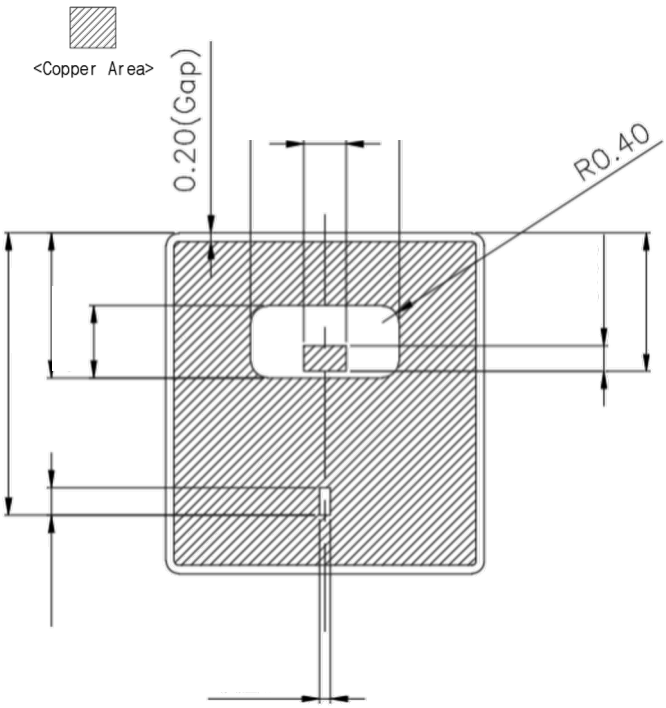
■ Copper layer 1 (Top)



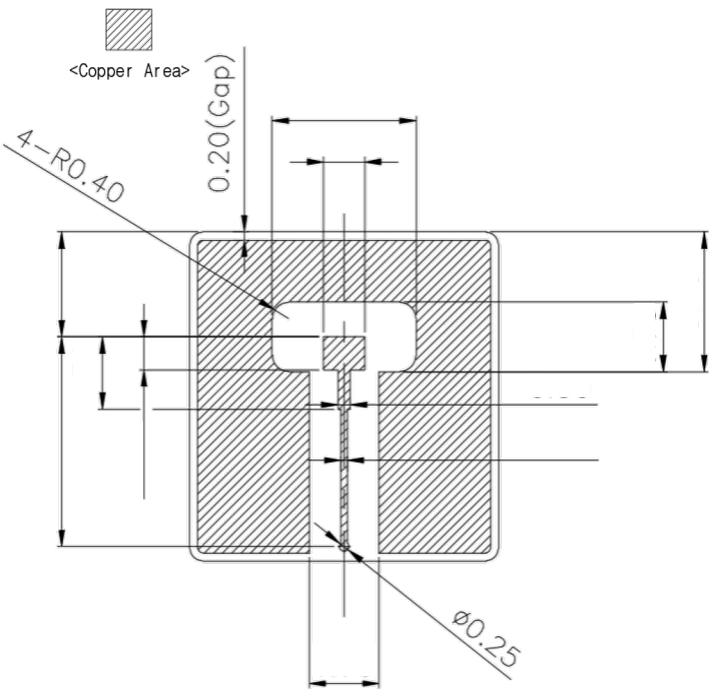
■ Copper layer 2



■ Copper layer 3



■ Copper layer 4 (Bottom)



PCB layer (Single)

■ PSR (Top)

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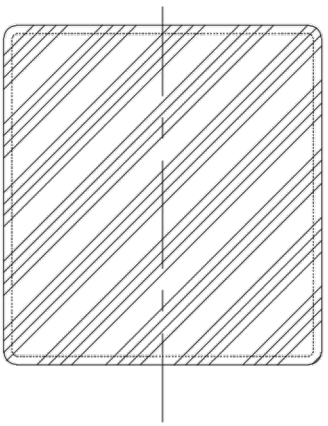
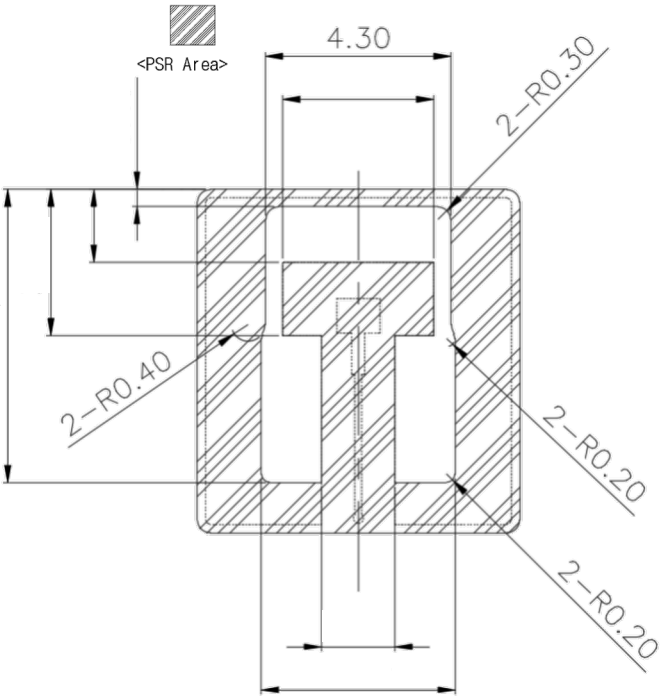


■ PSR (Bottom)

<PSR Area>



■ Solder paste (Bottom)

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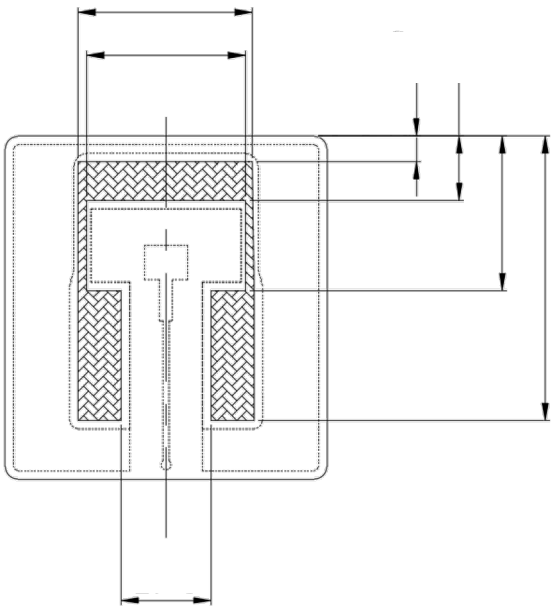
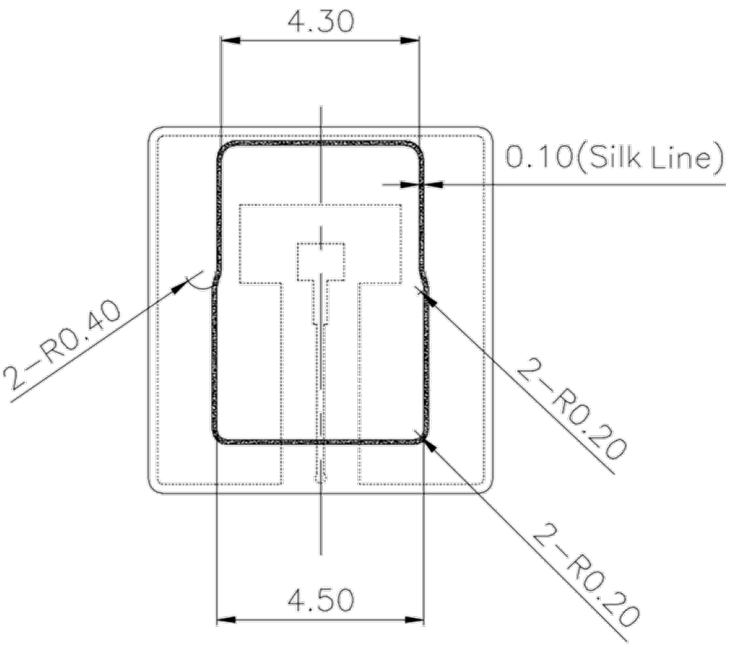


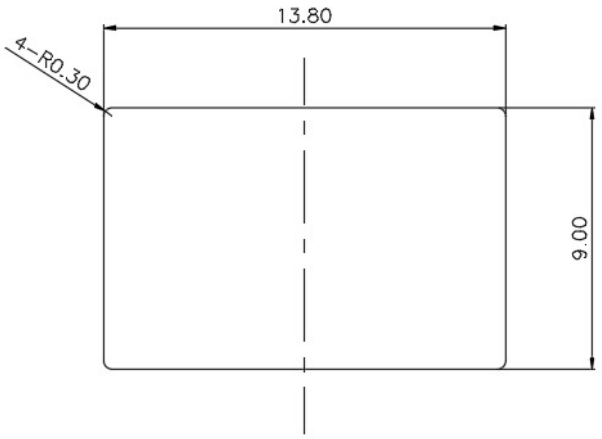
■ Silk screen printing (Bottom)

<Silk Screen Printing Area>

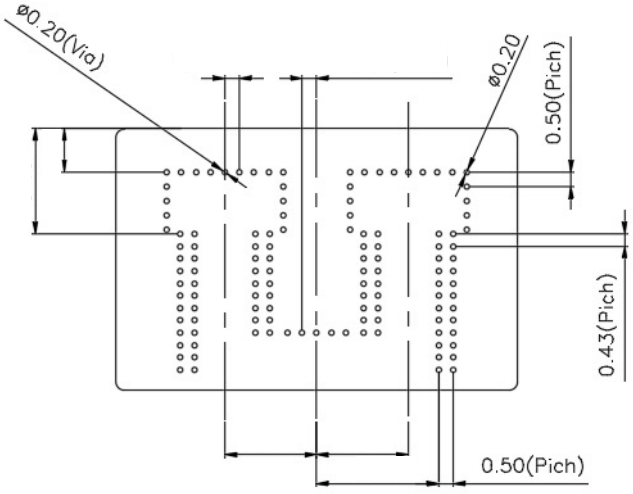


PCB layer (Dual)

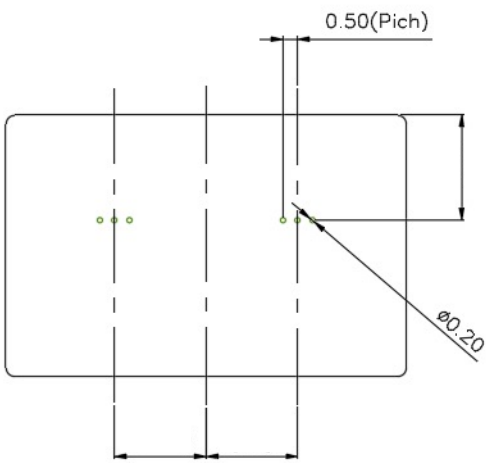
■ Contour



■ Via Hole (Layer 1 ~ Layer 4)

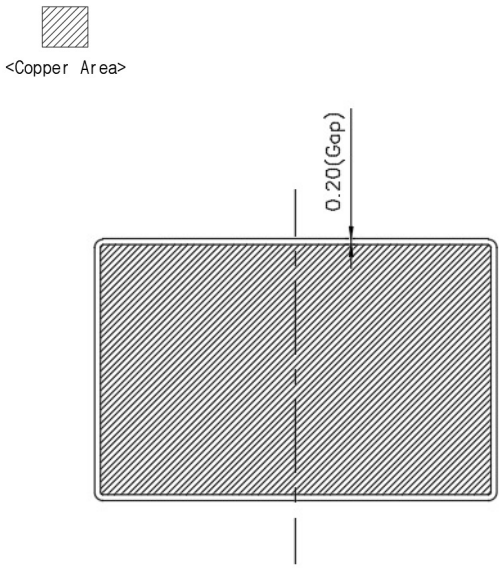


■ Via Hole (Layer 2 ~ Layer 3)

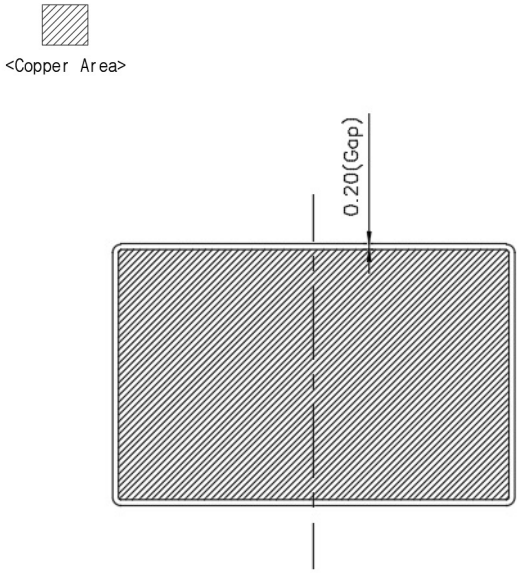


PCB layer (Dual)

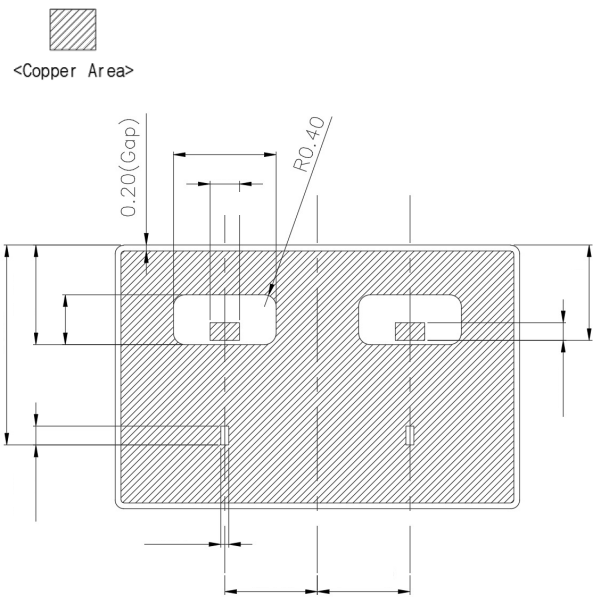
■ Copper layer 1 (Top)



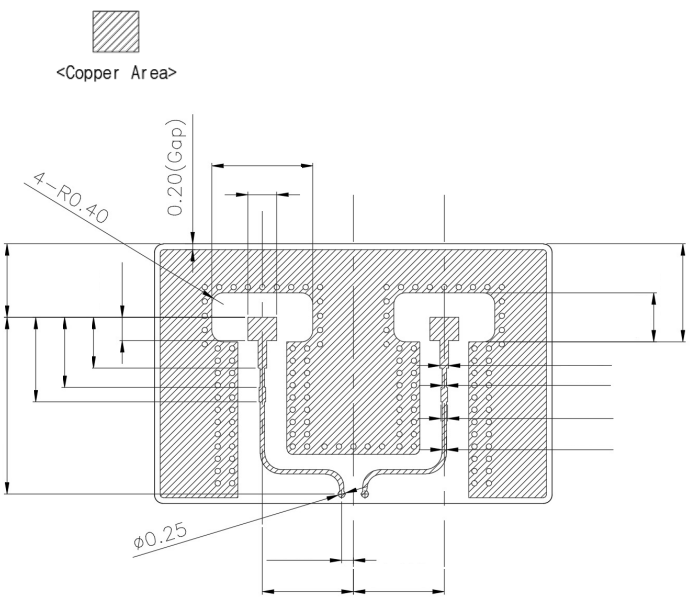
■ Copper layer 2



■ Copper layer 3



■ Copper layer 4 (Bottom)



PCB layer (Dual)

■ PSR (Top)

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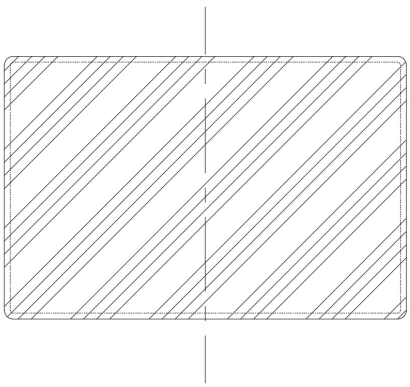
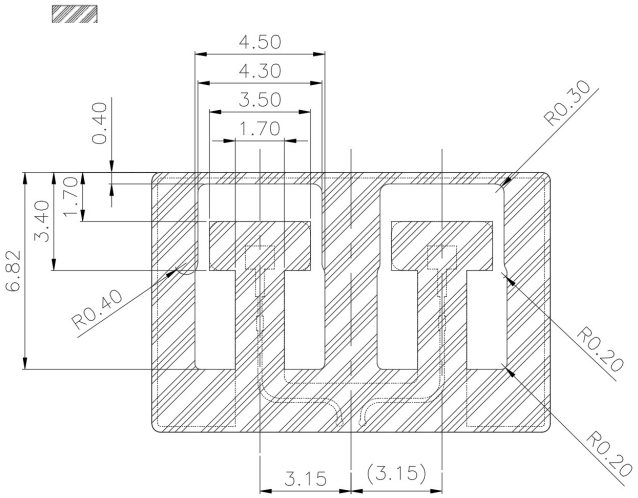


■ PSR (Bottom)



■ Solder paste (Bottom)

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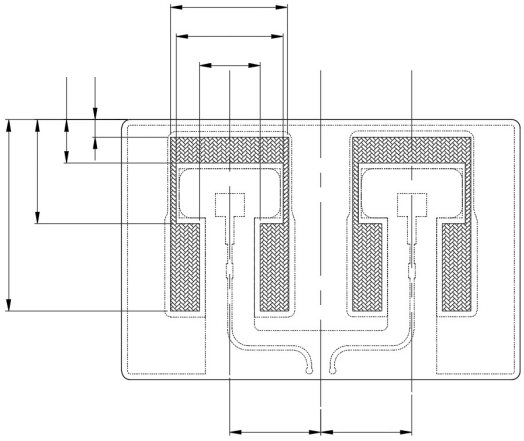

■ Silk screen printing (Bottom)

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